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(54) **DETERMINING DESIGN COORDINATES FOR WAFER DEFECTS**

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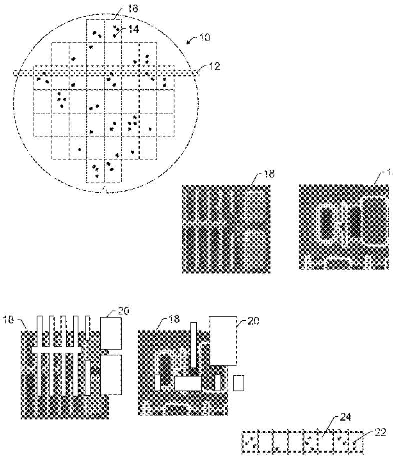
(57) **ABSTRACT**

Methods and systems for determining design coordinates for defects detected on a wafer are provided. One method includes aligning a design for a wafer to defect review tool images for defects detected in multiple swaths on the wafer by an inspection tool, determining a position of each of the defects in design coordinates based on results of the aligning, separately determining a defect position offset for each of the multiple swaths based on the swath in which each of the defects was detected (swath correction factor), the design coordinates for each of the defects, and a position for each of the defects determined by the inspection tool, and determining design coordinates for the other defects detected in the multiple swaths by the inspection tool by applying the appropriate swath correction factor to those defects.

27 Claims, 2 Drawing Sheets



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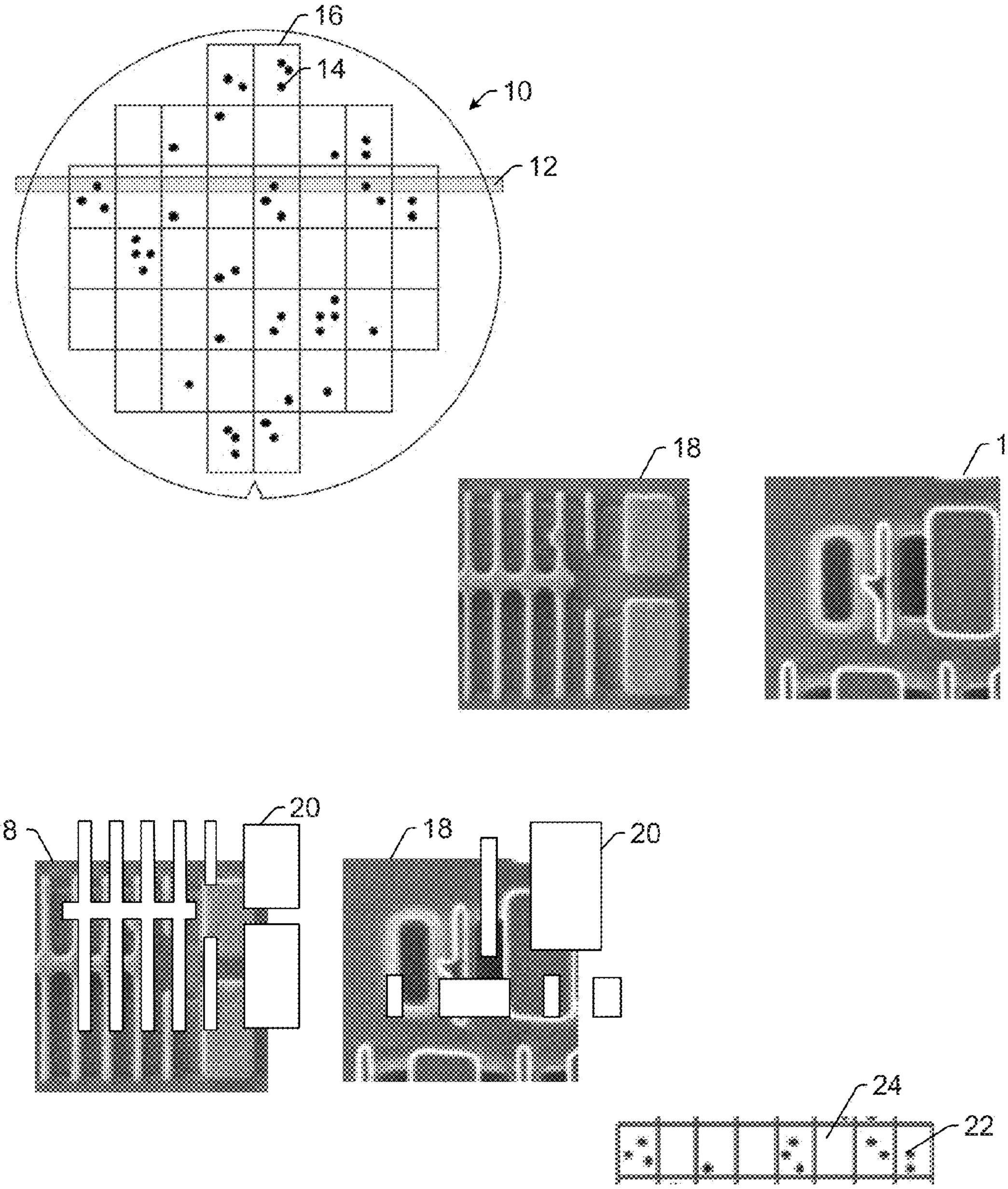
16
14
10
12
18
18
18
20
18
20
24
22

Fig. 1

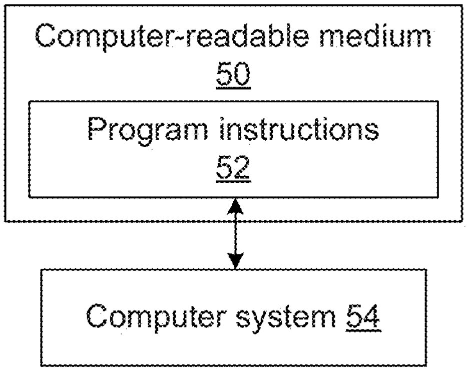
Computer-readable medium 50
Program instructions 52
Computer system 54

Fig. 2

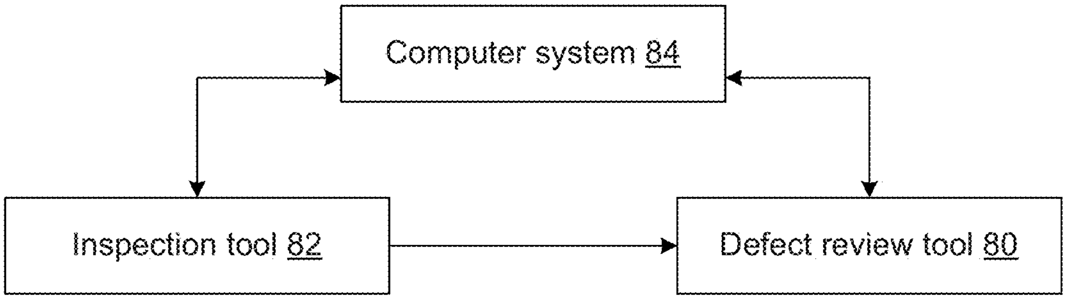
Computer system 84
Inspection tool 82
Defect review tool 80

Fig. 3

DETERMINING DESIGN COORDINATES FOR WAFER DEFECTS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. Provisional Application No. 61/534,104 entitled "1-Pixel Defect Location Accuracy (DLA) Through SEM Image Based Analysis and Cross Platform Integration," filed Sep. 13, 2011, which is incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to methods and systems for determining design coordinates for defects detected on a wafer.

2. Description of the Related Art

The following description and examples are not admitted to be prior art by virtue of their inclusion in this section.

Inspection processes are used at various steps during a semiconductor manufacturing process to detect defects on wafers to promote higher yield in the manufacturing process and thus higher profits. Inspection has always been an important part of fabricating semiconductor devices. However, as the dimensions of semiconductor devices decrease, inspection becomes even more important to the successful manufacture of acceptable semiconductor devices because smaller defects can cause the devices to fail.

Accurately determining the location of a defect on a wafer is important for a number of reasons. In currently used approaches, defect location accuracy is limited due to inspection tool capability such as stage accuracy and run-time alignment. Relative to locations in design, a wafer coordinate system can be manually aligned to a design coordinate system by compensating for differences in offset, scale, and rotation. However, this approach does not address the errors coming from swath-related location errors. As a result, defect location accuracy (DLA) is limited to several times the inspection pixel being used even on advanced inspection tools.

The manual method described above has many disadvantages. For example, DLA is only improved by manually aligning the wafer coordinate system to the design coordinate system. The correction is typically limited to two sites for the whole wafer and therefore it lacks consideration for swath-based error. DLA error includes both inspection tool error and design-to-wafer alignment error, thereby limiting the DLA error to several multiples of inspection pixel size.

Accordingly, it would be advantageous to develop systems and/or methods that do not have one or more of the disadvantages described above.

SUMMARY OF THE INVENTION

The following description of various embodiments is not to be construed in any way as limiting the subject matter of the appended claims.

One embodiment relates to a computer-implemented method for determining design coordinates for defects detected on a wafer. The method includes aligning a design for a wafer to images generated by a defect review tool for defects detected in multiple swaths by an inspection tool. The defects include two or more defects detected in each of the multiple swaths. In other words, in this method, two or more defects from each of the multiple swaths are aligned to the design. The method also includes determining a position of each of the defects in design coordinates based on results of the aligning step. In addition, the method includes separately determining a defect position offset for each of the multiple swaths based on the swath in which each of the defects was detected (defects that were detected and aligned from that swath), the design coordinates for each of the defects, and a position for each of the defects as determined by the inspection tool (the original wafer position). This produces a correction factor for each swatch. The method further includes determining design coordinates for other defects detected in the multiple swaths by the inspection tool by applying one of the defect position offsets to positions of the other defects determined by the inspection tool depending on the swath in which the other defects were detected (applying the appropriate swatch correction factor to the defect). The aligning step, determining the position, separately determining the swath-relative defect position offsets, and determining the design coordinates are performed by a computer system.

The method described above may be performed as described further herein. In addition, the method described above may include any other step(s) of any other method(s) described herein. Furthermore, the method described above may be performed by any of the systems described herein.

Another embodiment relates to a non-transitory computer-readable medium storing program instructions executable on a computer system for performing a computer-implemented method for determining design coordinates for defects detected on a wafer. The computer-implemented method includes the steps of the method described above. The computer-readable medium may be further configured as described herein. The steps of the computer-implemented method may be performed as described further herein. In addition, the computer-implemented method for which the program instructions are executable may include any other step(s) of any other method(s) described herein.

An additional embodiment relates to a system configured to determine design coordinates for defects detected on a wafer. The system includes a defect review tool configured to generate images for defects detected in multiple swaths scanned on a wafer by an inspection tool. The imaged defects include two or more defects detected in each of the multiple swaths. The system also includes a computer system configured to perform the steps of the method described above. The system may be further configured as described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

FIG. **1** is a schematic diagram illustrating one embodiment of a method for determining design coordinates for defects detected on a wafer;

FIG. **2** is a block diagram illustrating one embodiment of a non-transitory computer-readable medium that includes program instructions executable on a computer system for performing one or more of the computer-implemented methods described herein; and

FIG. **3** is a schematic diagram illustrating a side view of one embodiment of a system configured to determine design coordinates for defects detected on a wafer.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning now to the drawings, it is noted that the figures are not drawn to scale. In particular, the scale of some of the elements of the figures is greatly exaggerated to emphasize characteristics of the elements. It is also noted that the figures are not drawn to the same scale. Elements shown in more than one figure that may be similarly configured have been indicated using the same reference numerals.

One embodiment relates to a computer-implemented method for determining design coordinates for defects detected on a wafer. The embodiments described herein integrate several scattered technologies to improve defect locations after inspection. For example, the method includes aligning a design for a wafer to images generated by a defect review tool for defects detected in multiple swaths scanned on the wafer by an inspection tool. Therefore, the embodiments described herein effectively integrate inspection, defect review, and design technologies.

The method may or may not include running a defect inspection. For example, the method may include inspecting the wafer by scanning multiple swaths on the wafer using the inspection tool. Alternatively, information for the defects detected in the multiple swaths may be acquired for use in the methods described herein from a computer-readable storage medium in which the information has been stored by the inspection tool. In either case, the results of the wafer inspection may include an inspection results file. The inspection results file may be sent to the defect review tool so that the defect review tool may perform one or more steps described herein using information about the defects in the inspection results file. In a similar manner, the method may or may not include generating the images using the defect review tool. For example, the method may include imaging the detects on the wafer using the defect review tool. Alternatively, images generated by the defect review tool for the defects may be acquired for use in the methods described herein from a computer-readable storage medium in which the images have been stored by the defect review tool. The multiple swaths may include all or each of the swaths scanned on the wafer. In this manner, the method may include inspection swath-based alignment to improve defect location accuracy (DLA) for each swath.

In one embodiment, the design is provided in a Graphical Data System (GDS) or Open Artwork System Interchange Standard (OASIS) file. In another embodiment, the method includes acquiring the design from an electronic design automation (EDA) tool. In this manner, the method may include using defect review tool images and design layout for accurate alignment. The design or information for the design used in the embodiments described herein may include any other design data known in the art.

In one embodiment, the defect review tool is a scanning electron microscope (SEM). The SEM may include any suitable commercially available SEM defect review tool known in the art such as the eDR7000, which is commercially available from KLA-Tencor, Milpitas, Calif. In this manner, aligning the design to images generated by the defect review tool may include aligning SEM images to the design. Using SEM image-to-design alignment mitigates any inspection tool noise impact on the results produced by the embodiments described herein.

In another embodiment, the inspection tool is an optical (i.e., light-based) inspection tool. In some embodiments, the inspection tool is an electron beam-based inspection tool. The inspection tool may include any suitable commercially available light- or electron beam-based inspection tool known in the art. In addition, the light-based inspection tool may be a bright field (BF) and/or dark field (DF) inspection tool. In this manner, the inspection tool used in the embodiments described herein is not limited to BF, DF, and/or electron beam inspection. In other words, the embodiments described herein are independent of the inspection tool platform.

The defects include two or more defects detected in each of the multiple swaths. For example, the method may include using two defects per swath to align to design images. In one embodiment, the method includes sampling the defects for which the images are generated by the defect review tool based on the swath in which the defects are detected. For example, sampling the defects may include selecting a relatively small number of defects from each swath in an inspection tot result using swath information that is saved in the inspection results file. In this manner, the method may include inspection swath-based sampling to improve DLA for each swath. The two or more defects also preferably include fewer than all of the defects detected in each of the multiple swaths. The number of defects for which defect review tool images are generated in the embodiments described herein may vary depending on the speed of the defect review tool. For example, with faster defect review tool image generation, the same concept can be extended to include additional defects for even better accuracy and robustness.

in one such embodiment, as shown in FIG. **1**, wafer map **10** shows results of an inspection in which multiple swaths **12** were scanned on a wafer by an inspection tool (not shown in FIG. **1**), which detected defects **14** on the wafer. The wafer map also shows the locations of dies **16** on the wafer. Only one of the multiple swaths **12** is shown in FIG. **1** for simplicity. In this example, sampling the defects as described above may include sampling two defects per swath from the inspection results file post inspection. More specifically, two defects may be sampled from the swath shown in FIG. **1**, then two other defects may be sampled from another of the multiple swaths, and so on. After the defects have been sampled from the swaths on a swath-by-swath basis, images **18** may be generated for the sampled defects using the defect review tool (not shown in FIG. **1**) or may be acquired from a computer-readable storage medium in which the images have been stored by the defect review tool. As shown in FIG. **1**, images **18** may be relatively high resolution SEM images. The images may be generated by the defect review tool at the locations of the defects as determined by the inspection tool (e.g., at defect locations Xi, Yi). The aligning step may then include aligning images **18** to portions **20** of the design. The portions of the design may be called design "clips" or GDS clips.

In some embodiments, the method includes locating the defects in the images using automatic defect locating (ADL) performed by the defect review tool. For example, once the defects are imaged on the defect review tool, the defects may be located in the images by ADL. ADL may be performed in any suitable manner known in the art.

In one embodiment, the aligning includes image processing. In some embodiments, the image processing may include optimizing SEM images for best edge detection for each layer on the wafer. Such training may be automated. In another embodiment, the aligning step includes overlaying portions of the design with the images. In this manner, the aligning step may include overlaying SEM images with a design layout.

For example, as shown in FIG. **1**, images **18** may be overlaid with portions **20** of the design, and then the positions of images **18** relative to portions **20** of the design may be altered until features in the images substantially match features in the portions of the design.

The method also includes determining a position of each of the defects in design coordinates based on results of the aligning step. In this manner, the method includes determining defect design coordinates. For example, the defect location determined by ADL in the defect review tool-generated images may be assigned the design coordinates of the corresponding location in the design that overlays the detect after alignment. In this manner, the method may include determining substantially precise locations of the defects in design space with SEM location accuracy.

The method also includes separately determining a defect position offset for each of the multiple swaths (i.e. swatch correction factor) based on the swath in which each of the defects was detected, the design coordinates for each of the defects, and a position for each of the defects determined by the inspection tool. In this manner, the method may include determining a location correction for each of the multiple swaths. For example, the location correction for each of the multiple swaths may be determined based on the alignment to design coordinates.

The method further includes determining design coordinates for other defects detected in the multiple swaths by the inspection tool by applying one of the defect position offsets to positions of the other defects determined by the inspection tool depending on the swath in which the other defects were detected (i.e., applying the appropriate swath correction factor to each of the other defects detected from that swath). In this manner, the method includes applying the offsets to wafer inspection coordinates on a swath-by-swath basis to determine adjusted defect locations (e.g., corrected locations (Xf, Yf)). For example, as described above, two defects may be used to generate a location correction that may then be applied to all other defects in the multiple swaths on a swath-by-swath basis. In addition, the method includes image-based precision DLA. As such, a defect coordinate adjustment may be made from a SEM image to design file alignment. For example, the location corrections for each of the multiple swaths may be applied to all defects in the swaths on a swath-by-swath basis. In this manner, defect locations can be adjusted to improve the accuracy of the defect positions relative to the design.

The corrected defect locations may be sent to an inspection results file. For example, the results may be sent back to the inspection results file for further analysis. The corrected locations (Xf, Yf) can be used to enable new applications as well as to improve context based inspection (CBI) operation. CBI may be performed as described in U.S. Pat. No. 7,676,077 to Kulkarni et al., which is incorporated by reference as if fully set forth herein.

Aligning the design, determining the position, separately determining the defect position offset, and determining the design coordinates are performed by a computer system, which may be configured as described further herein.

In one embodiment, the defects and the other defects include all defects detected on the wafer. In other words, the defects used to determine the swath correction factor and the defects to which the appropriate swath correction factor is applied may include all defects on the wafer. In this manner, the design coordinates can be determined for all defects detected on the wafer. For example, as shown in FIG. **1**, corrected locations (Xf, Xy) may be determined for all defects **22** in dies **24** on a wafer in addition to all other defects in all other dies on the wafer.

In some embodiments, aligning the design, determining the position, separately determining the defect position offset, and determining the design coordinates produce design coordinates for the other defects that are accurate to within one pixel of the inspection tool. For example, the embodiments described herein provide 1-pixel DIA through SEM image-based analysis and cross-platform integration. In particular, the embodiments provide +/−1 inspection pixel coordinate accuracy for all defects in a wafer inspection result by sampling a relatively small subset of the defects on a SEM review tool. In this manner, the embodiments described herein overcome the multiple pixels accuracy limitation of inspection tools by aligning to design and revising defect position within defect review tool location accuracy (e.g., ADL accuracy) for the sampled defects. Such improvements enable new applications that would further the use of inspection and review tools. In addition, the defect locations from inspection can be improved as described herein without further improvement in the inspection tool performance. No other technology currently available can achieve this coordinate accuracy.

In another embodiment, aligning the design, determining the position, separately determining the defect position offset, and determining the design coordinates produce design coordinates for the other defects with an accuracy approximately equal to the accuracy of the defect review tool for determining the location of the defects within the images. For example, the defect locations from inspection can be altered as described herein to achieve DLA coordinate accuracy within the margin of the defect review tool location error (e.g., within about 6 nm for the eDR7000 system). In particular, the stage jitter for each swath is about one half of a pixel. Advanced Bright-Field tool today may be about 10 nm. Therefore, the embodiments described herein may provide about 6 nm accuracy for sampled defects and about 10 nm for other defects. No other technology currently available can achieve this level of coordinate accuracy.

The embodiments described herein may also include using defect review tool and design based alignment to feedback into an inspection results file for new use case development. For example, in one embodiment, the method includes selecting a bitmap pixel (aka defective pixel) in inspection results produced by the inspection tool for the wafer based on the design coordinates determined for one of the defects or the other defects and altering a process used to inspect the wafer based on the selected (defective) pixel. In this manner, the method may include the use of improved DLA to identify a single pixel that is impacted by a defect for inspection optimization. Such embodiments may be used for inspection sensitivity optimization for certain defects. For example, the method may result in the detection of previously undetected "gap" defects on the wafer. In addition, the method may include adjusting the offset for each defect using the defect review tool images. The method may also include applying corrected defect coordinates to determine the bitmap or defective pixel on which to base the inspection optimization.

In addition, the embodiments may include performing subpixel analysis to understand defect-to-defect behavior based on different defect types. The embodiments described herein may also be used for setting up CBI, some examples of which are described in the above-referenced patent to Kulkarni. For example, the methods described herein may include performing a hot scan on the wafer to detect more defects on the wafer. The design coordinates determined for the defects as described herein may then be used to identify hot spots in the design. For example, the design coordinates of defects that are the same as or near critical features in the design may be identified as hot spots in the design. Based on the identified hot spots, a CBI process can be set up for other wafers on which the design will be printed. For example, the CBI process can be set up such that the hot spots are inspected with higher sensitivity than non-hot spots on the wafer.

There are also a number of other potential applications of the approaches described herein possibly with further improvements in inspection. For example, the results of the methods described herein may be used for inline bitmapping (for DRAM, FLASH, and SRAM) to localize the defect to a particular memory cell. The results of the methods may also be used for sampling based on schematic overlay with defect (e.g., if a defect overlaps with a metal interconnect specified in the design, that defect may be sampled). In addition, the results of the methods described herein may be used for binning defects by single via or double via, for N/P transistor separation, for yield prediction for future layers (e.g., particle on contact), and for binning defects by short or broken line or on or in between lines.

The embodiments described herein have a number of advantages over currently used methods for determining defect locations. For example, previously used approaches apply a wafer level offset for design-to-wafer alignment. Using the previous approach, DLA is limited to manually aligning to design and inspection system error. In addition, an alternative approach would be to align relatively high resolution optical patch images of the defects generated by the inspection tool during inspection of the wafer to a design layout for real-time alignment. However, this approach requires reliable patch images and also requires a new image matching algorithm. In contrast, defect review tool images such as SEM images generally have much better pattern fidelity compared to optical images. As such, by aligning the defect review tool images to design using image processing, accurate alignment of defect-to-design can be achieved and therefore overall DLA is improved.

Each of the embodiments of the method described above may include any other step(s) of any other method(s) described herein. Furthermore, each of the embodiments of the method described above may be performed by any of the systems described herein.

All of the methods described herein may include storing results of one or more steps of the method embodiments in a computer-readable storage medium. The results may include any of the results described herein and may be stored in any manner known in the art. The storage medium may include any storage medium described herein or any other suitable storage medium known in the art. After the results have been stored, the results can be accessed in the storage medium and used by any of the method or system embodiments described herein, formatted for display to a user, used by another software module, method, or system, etc.

An additional embodiment relates to a non-transitory computer-readable medium storing program instructions executable on a computer system for performing a computer-implemented method for determining design coordinates for defects detected on a wafer. One such embodiment is shown in FIG. **2**. In particular, as shown in FIG. **2**, computer-readable medium **50** includes program instructions **52** executable on computer system **54**. The computer-implemented method includes the steps of the method described above. The computer-implemented method for which the program instructions are executable may include any other step(s) described herein.

Program instructions **52** implementing methods such as those described herein may be stored on computer-readable medium **50**. The computer-readable medium may be a storage medium such as a magnetic or optical disk, or a magnetic tape or any other suitable non-transitory computer-readable medium known in the art.

The program instructions may be implemented in any of various ways, including procedure-based techniques, component-based techniques, and/or object-oriented techniques, among others. For example, the program instructions may be implemented using ActiveX controls, C++ objects, JavaBeans, Microsoft Foundation Classes ("MFC"), or other technologies or methodologies, as desired.

The computer system may take various forms, including a personal computer system, image computer, mainframe computer system, workstation, network appliance, Internet appliance, or other device. In general, the term "computer system" may be broadly defined to encompass any device having one or more processors, which executes instructions from a memory medium. The computer system may also include any suitable processor known in the art such as a parallel processor. In addition, the computer system may include a computer platform with high speed processing and software, either as a standalone or a networked tool.

An additional embodiment relates to a system configured to determine design coordinates for defects detected on a wafer. One embodiment of such a system is shown in FIG. **3**. The system includes defect review tool **80** configured to generate images for defects detected in multiple swaths scanned on a wafer by inspection tool **82**. The defects include two or more defects detected in each of the multiple swaths, Defect review tool **80** and inspection tool **82** may be further configured as described herein. As shown in FIG. **3**, the defect review toot and the inspection tool may be coupled in some manner such that the inspection toot can send information about the defects to the defect review tool. For example, the inspection tool and the defect review tool may be coupled by a transmission medium (not shown), which may include wired and/or wireless portions, across which the inspection tool can send information to the defect review tool. Alternatively, the inspection tool may be effectively coupled to the defect review tool by a computer-readable storage medium (not shown in FIG. **3**) such as a fab database in which the inspection tool can store information for the defects and from which the defect review tool can retrieve the defect information.

The system also includes computer system **84** configured for aligning a design for the wafer to the images, which may be performed as described herein. The computer system is also configured for determining a position of each of the defects in design coordinates based on results of the aligning step, which may be performed as described further herein. In addition, the computer system is configured for separately determining a defect position offset for each of the multiple swaths based on the swath in which each of the defects was detected, the design coordinates for each of the defects, and a position for each of the defects determined by the inspection tool, which may be performed as described herein. The computer system is further configured for determining design coordinates for other defects detected in the multiple swaths by the inspection tool by applying one of the defect position offsets to positions of the other defects determined by the inspection tool depending on the swath in which the other defects were detected (applying the appropriate swath correction factor to those defects), which may be performed as described further herein.

The computer system may be coupled to the defect review toot and the inspection tool in a manner such as that described above such that the computer system can send and receive information to and from the defect review tool and the inspection tool. The computer system may also be coupled to other tools in a similar manner such as an EDA tool from which the design may be acquired by the computer system for use in the embodiments described herein. The computer system and the system may be configured to perform any other step(s) described herein and may be further configured as described herein.

Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. For example, methods and systems for determining design coordinates for defects detected on a wafer are provided. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments. Elements and materials may be substituted for those illustrated and described herein, parts and processes may be reversed, and certain features of the invention may be utilized independently, all as would be apparent to one skilled in the art after having the benefit of this description of the invention. Changes may be made in the elements described herein without departing from the spirit and scope of the invention as described in the following claims.

What is claimed:

1. A computer-implemented method for determining design coordinates for defects detected on a wafer, comprising:

aligning a design for a wafer to images generated by a defect review tool at locations of defects on the wafer, wherein the defects are detected in multiple swaths scanned on the wafer by a wafer inspection tool prior to said aligning and prior to generation of the images by the defect review tool, wherein the locations of the defects at which the defect review tool generates the images are determined by the wafer inspection tool, wherein the defects comprises two or more first defects detected in a first of the multiple swaths and two or more second defects detected in a second of the multiple swaths, and wherein said aligning comprises overlaying portions of the design with the images generated by the defect review tool at the locations of the defects on the wafer;

determining a position of each of the defects in design coordinates based on results of said aligning;

separately determining at least a first defect position offset for the first of the multiple swaths, based on the design coordinates for each of the first defects and a position for each of the first defects determined by the wafer inspection tool, and a second defect position offset for the second of the multiple swaths, based on the design coordinates for each of the second defects and a position for each of the second defects determined by wafer inspection tool; and

determining design coordinates for other defects detected in the multiple swaths by the wafer inspection tool by applying the first defect position offset to positions of the other defects determined by the wafer inspection tool that were detected in the first of the multiple swaths and applying the second defect position offset to positions of the other defects determined by the wafer inspection tool that were detected in the second of the multiple swaths, wherein said aligning, determining the position, separately determining at least the first and second defect position offsets, and determining the design coordinates are performed by a computer system.

2. The method of claim **1**, wherein the defects and the other defects comprise all defects detected on the wafer.

3. The method of claim **1**, wherein said aligning, determining the position, separately determining at least the first and second defect position offsets, and determining the design coordinates produce design coordinates for the other defects that are accurate to within one pixel size of a pixel used by the wafer inspection tool when inspecting the wafer.

4. The method of claim **1**, wherein said aligning, determining the position, separately determining at least the first and second defect position offsets, and determining the design coordinates produce design coordinates for the other defects that have an accuracy approximately equal to an accuracy of the defect review tool for determining a location of the defects within the images.

5. The method of claim **1**, wherein the design is provided in a Graphical Data System (GDS) or Open Artwork System Interchange Standard (OASIS) file.

6. The method of claim **1**, further comprising acquiring the design from an electronic design automation (EDA) tool.

7. The method of claim **1**, wherein the defect review tool is a scanning electron microscope.

8. The method of claim **1**, wherein the wafer inspection tool is an optical inspection tool.

9. The method of claim **1**, wherein the wafer inspection tool is an electron beam-based inspection tool.

10. The method of claim **1**, further comprising sampling the defects for which the images are generated by the defect review tool based on the swath in which the defects are detected.

11. The method of claim **1**, further comprising locating the defects in the images using automatic defect locating performed by the defect review tool.

12. The method of claim **1**, wherein said aligning further comprises image processing.

13. The method of claim **1**, further comprising selecting a bitmap pixel in inspection results produced by the wafer inspection tool for the wafer based on the design coordinates determined for one of the defects or the other defects and altering a process used to inspect the wafer based on the selected pixel.

14. A non-transitory computer-readable medium, storing program instructions executable on a computer system for performing a computer-implemented method for determining design coordinates for defects detected on a wafer, wherein the computer-implemented method comprises:

aligning a design for a wafer to images generated by a defect review tool at locations of defects on the wafer, wherein the defects are detected in multiple swaths scanned on the wafer by a wafer inspection tool prior to said aligning and prior to generation of the images by the defect review tool, wherein the locations of the defects at which the defect review tool generates the images are determined by the wafer inspection tool, wherein the defects comprise two or more first defects detected in a first of the multiple swaths and two or more second defects detected in a second of the multiple swaths, and wherein said aligning comprises overlaying portions of the design with the images generated by the defect review tool at the locations of the defects on the wafer;

determining a position of each of the defects in design coordinates based on results of said aligning;

separately determining at least a first defect position offset for the first of the multiple swaths, based on the design coordinates for each of the first defects and a position for each of the first defects determined by the wafer inspection tool, and a second defect position offset for the second of the multiple swaths, based on the design coordinates for each of the second defects and a position for each of the second defects determined by the wafer inspection tool; and

determining design coordinates for other defects detected in the multiple swaths by the wafer inspection tool by applying the first defect position offsets to positions of the other defects determined by the wafer inspection tool that were detected in the first of the multiple swaths and applying the second defect position offset to positions of the other defects determined by the wafer inspection tool that were detected in the second of the multiple swaths.

15. A system configured to determine design coordinates for defects detected on a wafer, comprising:

a defect review tool configured to generate images at locations of defects on the wafer, wherein the defects are detected in multiple swaths scanned on the wafer by a wafer inspection tool, wherein the locations of the defects at which the defect review tool generates the images are determined by the wafer inspection tool, and wherein the defects comprise two or more first defects detected in a first of the multiple swaths and two or more second defects detected in a second of the multiple swaths; and

a computer system configured for:

aligning a design for the wafer to the images, wherein the defects are detected by the wafer inspection tool prior to said aligning and prior to generation of the images by the defect review tool;

determining a position of each of the defects in design coordinates based on results of said aligning;

separately determining at least a first defect position offset for the first of the multiple swaths, based on the design coordinates for each of the first defects and a position for each of the first defects determined by the wafer inspection tool, and a second defect position offset for the second of the multiple swaths, based on the design coordinates for each of the second defects and a position for each of the second defects determined by the wafer inspection tool; and

determining design coordinates for other defects detected in the multiple swaths by the wafer inspection tool by applying the first defect position offsets to positions of the other defects determined by the wafer inspection tool that were detected in the first of multiple swaths and applying the second defect position offset to positions of the other defects determined by the wafer inspection tool that were detected in the second of the multiple swaths.

16. The system of claim **15**, wherein the defects and the other defects comprise all defects detected on the wafer.

17. The system of claim **15**, wherein said aligning, determining the position, separately determining at least the first and second defect position offsets, and determining the design coordinates produce design coordinates for the other defects that are accurate to within one pixel size of a pixel used by the wafer inspection tool when inspecting the wafer.

18. The system of claim **15**, wherein said aligning, determining the position, separately determining at least the first and second defect position offsets, and determining the design coordinates produce design coordinates for the other defects that have an accuracy approximately equal to an accuracy of the defect review tool for determining a location of the defects within the images.

19. The system of claim **15**, wherein the design is provided in a Graphical Data System (GDS) or Open Artwork System Interchange Standard (OASIS) file.

20. The system of claim **15**, wherein the computer system is further configured for acquiring the design from an electronic design automation (EDA) tool.

21. The system of claim **15**, wherein the defect review tool is a scanning electron microscope.

22. The system of claim **15**, wherein the wafer inspection tool is an optical inspection tool.

23. The system of claim **15**, wherein the wafer inspection tool is an electron beam-based inspection tool.

24. The system of claim **15**, wherein the computer system is further configured for sampling the defects for which the images are generated by the defect review tool based on the swath in which the defects are detected.

25. The system of claim **15**, wherein the detect review tool is further configured to locate the defects in the images using automatic defect locating.

26. The system of claim **15**, wherein said aligning further comprises image processing.

27. The system of claim **15**, wherein the computer system is further configured for selecting a bitmap pixel in inspection results produced by the wafer inspection tool for the wafer based on the design coordinates determined for one of the defects or the other defects and altering a process used to inspect the wafer based on the selected pixel.

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